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## **May 11th, 2018 - arithmetic core lphaAdditional info FPGA**

provenWishBone Compliant NoLicense LGPLDescriptionRTL Verilog code to perform Two Dimensional Fast Hartley Transform 2D FHT for 8x8 points Presented algorithm is FHT with decimation in frequency domain Main FeaturesHigh Clock SpeedLow Latency 97 clock cycles Low Slice CountSingle Clock Cycle per'

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May 10th, 2018 - S NO Paper Code List of Authors Paper Title Registration Status Registered Author's Certificate for Co Author Page No Presentation Date 51 051 Sabah Mazhir Aiyah Noori Alyaa Hussein and Hazm Ismail'

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