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'**Creating a custom IP block in Vivado FPGA Developer**

May 2nd, 2018 - Hi Natalie I had trouble with this at first too What you?re seeing is a Verilog file not a VHDL file You can fix this by changing the target language to VHDL'

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'**Intel FPGA HDMI IP Core User Guide Altera**

November 5th, 2017 - Information Description Release Information Version 17 1 Release November 2017 Ordering Code IP HDMI IP Core Information'

'**AES IP Core Ultra Compact Advanced Encryption Standard**

May 5th, 2018 - The AES core implements Rijndael cipher encoding and decoding in compliance with the NIST Advanced Encryption Standard It processes 128 bit data blocks with 128 bit key a 256 bit key version is available'

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'**Zilog Z80 Wikipedia**
May 2nd, 2018 - An early Z80 microprocessor manufactured in June 1976 according to the date stamp'
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